REMARKS

By the present amendment, claims 1, 7, 11-12, and 15 have been amended. Thus, claims 1-17 remain pending in the present application. Additionally, the specification has been amended. Reconsideration and allowance of pending claims 1-17 in view of the above amendments and following remarks are requested.

A. Rejection of Claim 1 under the Judicially Created Doctrine of Double Patenting

The Examiner has rejected claim 1 under the judicially created doctrine of double patenting as being unpatentable over claim 1 of co-pending U.S. Patent Application Number 09/586,325.Along with the present Amendment and Response, Applicant has submitted a terminal disclaimer to overcome the Examiner's rejection under the judicially created doctrine of double patenting with respect to claim 1 of co-pending U.S. Patent Application Number 09/586,325. Applicant respectfully submits that the enclosed terminal disclaimer overcomes the Examiner's double patenting rejection.

B. Objection to the Specification

The Examiner has objected to the specification as including an improper attempt to incorporate subject matter into the present application by reference. Applicant has amended the specification to correctly incorporate the subject matter in question.

Consequently, Applicant respectfully requests that the objection to the specification be withdrawn.

C. **Rejection of Claims 1-17 under 35 USC §102(b)**

The Examiner has rejected claims 1, 2, 7, 11-12, and 15 under 35 USC §102(b) as being anticipated by "Synthesis and Simulation of Digital Systems Containing Interacting Hardware and Software Components," by Gupta et al. ("Gupta"). The Examiner has rejected claims 1-17 under 35 USC §102(b) as being anticipated by U.S. Patent Number 5,615,357 to Ball, et al. ("Ball"). For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by amended independent claims 1, 7, 11-12, and 15, is patentably distinguishable over Gupta and Ball.

The present invention relates to digital design system verification. Previous attempts simulated both the hardware components and the software components of a system design having integrated hardware and software components. However, these attempts used a discrete logic simulator simulation environment for the hardware components and a discrete instruction set simulation environment for the software components.

Embodiments according to the present invention integrate the hardware and software components of a system design in a single unified simulation environment. In one illustrative embodiment, use of a system model in a unified simulation allows application software to be loaded into a memory component in the system model. For

example, a low level operating system application can be loaded into a memory component in the simulation environment. During simulation, a processor component of the system model can simulate the operation of the operating system application by executing the instructions of the operating system. This allows a single simulation environment to simulate both the hardware components (memory and processor) as well as a software component (the operating system application). (Present application, page 18, lines 1-8). One advantage of the unified simulation environment is that it runs as one process. Thus, simulation time is reduced and debugging is greatly simplified.

Applicant has amended independent claims 1, 7, 11-12, and 15 in order to further illustrate aspects of the present invention. Specifically, independent claims 1, 7, 11-12, and 15 recite language indicating that a unified simulation runs as a single process and allows a program (e.g. application program) to be loaded into a memory component for simulation.

In contrast, Gupta relates to the synthesis of systems containing both application-specific and re-programmable components (e.g. off-the-shelf microprocessors). Gupta teaches a simulator performing concurrent simulation of multiple functional models implemented either as a program or as application-specific hardware. Referring to Gupta, page 2, it is noted that "[t]he hardware component of the system design can be simulated either before or after the structural synthesis phase." In Gupta, simulation of hardware and software is performed separately. Gupta does not teach a unified simulation that runs

as a single process and allows an application program to be loaded into a memory component for simulation.

In contrast to the present invention as defined by amended independent claims 1, 7, 11-12, and 15, Ball teaches a system and method for verifying processor performance. The Examiner states that Ball discloses a unified simulation design/program product/method for simulating a system design in Figure 5A. However, Figure 5A and the corresponding text simply relate to a simulator employing a benchmark program to generate performance statistics. Figure 5A does not teach the unified simulation of the present invention.

Further, the Examiner asserts that Ball teaches, at column 6, lines 36-51, a step of the present invention of associating the software component with the programming model of the memory component within a simulation environment. However, Ball, at column 6, lines 36-51, merely discusses object oriented programming in an overview form. Ball does not teach a unified simulation that runs as a single process and allows an application program to be loaded into a memory component for simulation. Therefore, Gupta and Ball do not disclose, teach, or suggest the present invention as defined by amended independent claims 1, 7, 11-12, and 15.

For the foregoing reasons, Applicant respectfully submits that the present invention as defined by independent claims 1, 7, 11-12, and 15 is not taught, disclosed, or suggested by Gupta and Ball. Thus, independent claims 1, 7, 11-12, and 15 are patentably distinguishable over Gupta and Ball. As such, the claims depending from amended

independent claims 1, 7, 11-12, and 15 are, *a fortiori*, also patentably distinguishable over Gupta and Ball for at least the reasons presented above and also for additional limitations contained in each dependent claim.

D. Conclusion

Based on the foregoing reasons, the present invention, as defined by amended independent claims 1, 7, 11-12, and 15, and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, outstanding claims 1-17 are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early Notice of Allowance directed to claims 1-17 pending in the present application are respectfully requested.

Respectfully Submitted,
FARJAMI & FARJAMI LLP

Date: 6/23/04

Michael Farjami, Esq.
Reg. No. 38,135

FARJAMI & FARJAMI LLP
26522 La Alameda Ave., Suite 360
Mission Viejo, California 92691
Telephone: (949) 282-1000
Facsimile: (949) 282-1002

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